

CLAIMS

1. A system for reducing current leakage in a circuit comprising:
an electrical path susceptible to leakage in said integrated circuit and
means for selectively blocking said path via feedback within said integrated circuit to eliminate or reduce leakage through said path.
2. The system of Claim 1 wherein said means for selectively blocking includes:
a first circuit component in said path, which is between a relatively high voltage and a relatively low voltage; a second circuit component in said path; and means for selectively providing feedback from an output of said second circuit component to an input of said first circuit component to selectively cutoff said path at said first circuit when said path is not cutoff at said second circuit.
3. The system of Claim 2 wherein said means for selectively providing feedback further includes means for preserving data in said circuit.
4. The system of Claim 3 wherein said means for preserving data in said circuit includes means for selectively enabling said feedback when said circuit is in sleep mode.
5. The system of Claim 4 wherein said means for selectively enabling said feedback includes a multiplexer.
6. The system of Claim 5 wherein said multiplexer is a 2-1 multiplexer having a shift input as a control input and having a scan-in input as one input and said feedback as a second input.
7. The system of Claim 5 wherein said first circuit component is a first Complimentary Metal Oxide Semiconductor (CMOS) inverter, and wherein said second circuit component is a second CMOS inverter.

8. The system of Claim 7 wherein said feedback path is chosen so that when said feedback path is activated, a high state occurring at an input of said second CMOS inverter results in a high state at an input of said first CMOS inverter, and a low state occurring at an input of said second CMOS inverter results in a low state at an input of said first CMOS inverter.

9. The system of Claim 7 wherein said circuit is a master-slave latch.

10. The system of Claim 9 wherein when said latch sleeps when a synchronizing clock signal of said latch is high, additional logic shuts off leakage paths in a master cell of said latch via High Voltage Threshold (HVT) transistors that are positioned in a selectively gated inverter in said master cell.

11. The system of Claim 10 further including means for selectively disabling said feedback when said clock signal sleeps high, and wherein said additional logic is positioned to block any remaining unblocked leakage paths.

12. The system of Claim 11 further including means for blocking said path via said clock signal and an HVT pass gate positioned between said first circuit component and said second component when said clock signal sleeps high.

13. A high-performance, low-leakage latch comprising:

a clock signal;

a circuit containing transistors arranged so that data is selectively transferred from an input of said circuit to an output of said circuit in response to said clock signal; and

means for employing feedback within said circuit to block leakage paths through said transistors via one or more of said transistors when said circuit is in sleep mode.

14. The latch of Claim 13 wherein said circuit contains LVT and HVT transistors, and wherein said means for employing feedback within said circuit includes means for blocking leakage paths through LVT transistors in said circuit via one or more of said HVT transistors when said circuit is in sleep mode.

15. The latch of Claim 14 wherein said LVT transistors are arranged to minimize setup time and transition delay of said latch when said latch is in operating mode.

16. The latch of Claim 15 wherein said means for blocking leakage includes means for turning off said one or more HVT transistors when said circuit is in sleep mode.

17. The latch of Claim 16 wherein said circuit includes a master cell and a slave cell, said feedback occurring from said slave cell to said master cell.

18. The latch of Claim 17 wherein said feedback represents half-latch data from said slave cell.

19. The latch of Claim 18 further including a shift signal, said shift signal indicating when said circuit is in sleep mode.

20. The latch of Claim 15 wherein said latch lacks HVT pass gates in a data path from said input to said output and includes two LVT pass gates in said data path.

21. The latch of Claim 20 wherein one of said LVT pass gates is included in a master cell of said latch, and a second LVT pass gate is included in a slave cell of said latch.

22. The latch of Claim 21 wherein all leakage paths of said latch flow through off HVT transistors when said latch is in sleep mode.

23. The latch of Claim 22 further including means for automatically enabling said latch to sleep when said clock signal of said latch is high or low.

24. The system of Claim 23 wherein when said latch sleeps when said clock signal is high, additional logic shuts off leakage paths in said master cell via HVT transistors that are positioned in a selectively gated inverter in said master cell.

25. The system of Claim 24 further including means for selectively disabling said feedback when said clock signal sleeps high, and wherein said additional logic is positioned to block any remaining unblocked leakage paths.

26. The latch of Claim 23 wherein said means for automatically enabling includes a multiplexer in communication with a controller for selectively controlling said feedback.

27. The latch of Claim 26 wherein said multiplexer is integrated with said master cell.

28. The latch of Claim 23 wherein said synchronizing clock signal includes two synchronizing clock signals having different phases.

29. A high-performance, low-leakage latch comprising:

a circuit containing LVT and HVT transistors arranged so that data is selectively transferred from an input of said circuit to an output of said circuit in response to a clock signal, said circuit having LVT pass gates but lacking HVT pass gates in a data path between an input and an output of said circuit; and

means for employing feedback within said circuit to block leakage paths through said LVT transistors via one or more of said HVT transistors when said circuit is in sleep mode by selectively turning off said one or more HVT transistors in response to said feedback.

30. A method for reducing current leakage in a circuit comprising the steps of:

positioning a first circuit component in a path between a relatively high voltage and a relatively low voltage;

placing a second circuit component in said path; and

selectively providing feedback from an output of said second circuit component to an input of said first circuit component to selectively cutoff said path at said first circuit when said path is not cutoff at said second circuit.